

### IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (amended): A multilayer printed wiring board comprising:

a substrate [provided with] having at least one through-hole structure, [the substrate having] the at least one through-hole structure comprising a plated film and being filled with filler;

at least one interlaminar resin insulating layer formed [thereon] on the substrate; and

at least one conductor circuit formed on the at least one interlaminar resin insulating layer[, the at least one through-hole being filled with filler],

wherein [an internal] a surface of the plated film of the at least one through-hole structure is roughened, and the filler comprises metal particles and one of thermosetting and thermoplastic resin.

Claim 2: The multilayer printed wiring board according to claim 1, wherein the substrate is a multilayer core substrate formed by laminating at least one conductor layer and at least one prepreg in alternating order.

Claim 3 (amended): The multilayer printed wiring board according to claim 1, wherein at least one through-hole structure formed [on] in the substrate has a pitch interval of equal to or less than 700  $\mu\text{m}$ .

Claim 4 (amended): The multilayer printed wiring board according to claim 1, [comprising build-up wiring layers including at least one via-hole provided in the at least one interlaminar resin insulating layer] wherein the at least one interlaminar resin insulating layer comprises a plurality of interlaminar resin insulating layers, the plurality of interlaminar resin insulating layers and at least one via-hole provided in the interlaminar resin insulating layers form build-up wiring layers, and the build-up wiring layers are formed on both surfaces of the

substrate[, and have the same number of layers [with each other] on both surfaces of the substrate.

Claim 5 (amended): A multilayer printed wiring board comprising:  
a substrate [provided with] having at least one through-hole structure, [the substrate having] the at least one through-hole structure being filled with filler;  
at least one interlaminar resin insulating layer formed [thereon] on the substrate; and  
at least one conductor circuit formed on the at least one interlaminar resin insulating layer[, the at least one through-hole being filled with filler],

wherein an internal surface of the at least one through-hole structure is roughened,  
and the filler comprises particulate substance including metal particles having a particle size of from 0.1 to 30  $\mu\text{m}$ , resin, and ultrafine inorganic powder having a particle size from [1 to 1000] 2 to 100 nm.

Claim 6 (amended): The multilayer printed wiring board according to claim 5,  
wherein the filler is a nonconducting composition [containing metal particles].

Claim 7 (amended): The multilayer printed wiring board according to claim 5,  
wherein the particulate substance comprises at least one of [metal particles,] inorganic particles and resin particles.

Claim 8: The multilayer printed wiring board according to claim 5, wherein the resin comprises at least one of bisphenol epoxy resin and novolac epoxy resin.

Claim 9: The multilayer printed wiring board according to claim 5, wherein the substrate is a multilayer core substrate formed by laminating at least one conductor layer and at least one prepreg in alternating order.

Claim 10 (amended): The multilayer printed wiring board according to claim 5,  
wherein the at least one through-hole structure formed [on] in the substrate has a pitch interval of equal to or less than 700  $\mu\text{m}$ .

Claim 11 (amended): The multilayer printed wiring board according to claim 5, [comprising build-up wiring layers including at least one via-hole provided in the at least one interlaminar resin insulating layer] wherein the at least one interlaminar resin insulating layer comprises a plurality of interlaminar resin insulating layers, the plurality of interlaminar resin insulating layers and at least one via-hole provided in the interlaminar resin insulating layers form build-up wiring layers, and the build-up wiring layers are formed on both surfaces of the substrate[,], and have the same number of layers [with each other] on both surfaces of the substrate.

Claim 12 (amended): A multilayer printed wiring board comprising:  
a substrate [provided with] having at least one through-hole structure, [the substrate having] the at least one through-hole structure comprising a plated film and being filled with filler;

at least one interlaminar resin insulating layer formed [thereon] on the substrate; and  
at least one conductor circuit formed on the at least one interlaminar resin insulating layer[, the at least one through-hole being filled with filler],

wherein [an internal] a surface of the plated film of the at least one through-hole structure is roughened, [and] the filler comprises metal particles and one of thermosetting and thermoplastic resin, and an exposed portion of the filler in the at least one through-hole is covered with a [portion of the at least one conductor circuit] through-hole-covering conductor layer.

Claim 13 (amended): The multilayer printed wiring board according to claim 12, wherein [a roughened layer is formed on] a surface of the [at least one conductor circuit] through-hole-covering conductor layer covering at least the one through-hole structure is roughened.

Claim 14: The multilayer printed wiring board according to claim 12, wherein the substrate is a multilayer core substrate formed by laminating at least one conductor layer and at least one prepreg in alternating order.

Claim 15 (amended): The multilayer printed wiring board according to claim 12, wherein the at least one through-hole structure formed [on] in the substrate has a pitch interval of equal to or less than 700  $\mu\text{m}$ .

Claim 16 (amended): The multilayer printed wiring board according to claim 12, [comprising build-up wiring layers including the at least one via-hole provided in the at least one interlaminar resin insulating layer] wherein the at least one interlaminar resin insulating layer comprises a plurality of interlaminar resin insulating layers, the plurality of interlaminar resin insulating layers and at least one via-hole provided in the interlaminar resin insulating layers form build-up wiring layers, and the build-up wiring layers are formed on both surfaces of the substrate[, and have the same number of layers [with each other] on both surfaces of the substrate.

Claim 17 (amended): A multilayer printed wiring board comprising:  
a substrate [provided with] having at least one through-hole structure, [the substrate having] the at least one through-hole structure being filled with filler;  
at least one interlaminar resin insulating layer formed [thereon] on the substrate; and  
at least one conductor circuit formed on the at least one interlaminar resin insulating layer[, the at least one through-hole being filled with filler],

wherein an internal surface of the at least one through-hole structure is roughened, [and] the filler comprises particulate substance having a particle size of from 0.1 to 30  $\mu\text{m}$ , resin, and ultrafine inorganic powder having a particle size from [1 to 1000] 2 to 100 nm, and an exposed portion of the filler in the at least one through-hole structure is covered with a [portion of the at least one conductor circuit] through-hole-covering conductor layer.

Claim 18: The multilayer printed wiring board according to claim 17, wherein the filler is a nonconducting composition containing metal particles.

Claim 19: The multilayer printed wiring board according to claim 17, wherein the particulate substance comprises at least one of metal particles, inorganic particles and resin particles.

Claim 20: The multilayer printed wiring board according to claim 17, wherein the resin comprises at least one of bisphenol epoxy resin and novolac epoxy resin.

Claim 21 (amended): The multilayer printed wiring board according to claim 17, wherein [a roughened layer is formed on] a surface of the [at least one conductor circuit] through-hole-covering conductor layer covering the at least one through-hole structure is roughened.

Claim 22: The multilayer printed wiring board according to claim 17, wherein the substrate is a multilayer core substrate formed by laminating at least one conductor layer and at least one prepreg in alternating order.

Claim 23 (amended): The multilayer printed wiring board according to claim 17, wherein at least one through-hole structure formed [on] in the substrate has a pitch interval equal to or less than 700  $\mu\text{m}$ .

Claim 24 (amended): The multilayer printed wiring board according to claim 17, [comprising build-up wiring layers including the at least one via-hole provided in the at least one interlaminar resin insulating layer] wherein the at least one interlaminar resin insulating layer comprises a plurality of interlaminar resin insulating layers, the plurality of interlaminar resin insulating layers and at least one via-hole provided in the interlaminar resin insulating layers form build-up wiring layers, and the build-up wiring layers are formed on both surfaces of the substrate[,], and have the same number of layers [with each other] on both surfaces of the substrate.

Claim 25 (amended): A multilayer printed wiring board comprising:  
a substrate [provided with] having at least one through-hole structure, [the substrate having] the at least one through-hole structure comprising a plated film and being filled with filler;

at least one interlaminar resin insulating layer formed [thereon] on the substrate; and  
at least one conductor circuit formed on the at least one interlaminar resin insulating layer[, the at least one through-hole structure being filled with filler],

wherein [an internal] a surface of the plated film of the at least one through-hole structure is roughened, [and] the filler comprises metal particles and one of thermosetting and thermoplastic resin, [and] an exposed surface of the filler in the at least one through-hole structure is covered with a [portion of the at least one conductor circuit] through-hole-covering conductor layer, and at least one viahole is formed in the at least one interlaminar resin insulating layer [just] directly above the [at least one conductor circuit and is connected to the at least one conductor circuit] through-hole-covering conductor layer.

Claim 26 (amended): The multilayer printed wiring board according to claim 25, wherein a [roughened layer is formed on] surface of the through-hole-covering conductor layer is roughened.

Claim 27: The multilayer printed wiring board according to claim 25, wherein the substrate is a multilayer core substrate formed by laminating at least one conductor layer and at least one prepreg in alternating order.

Claim 28 (amended): The multilayer printed wiring board according to claim 25, wherein the at least one through-hole structure formed [on] in the substrate has a pitch interval of equal to or less than 700  $\mu\text{m}$ .

Claim 29 (amended): The multilayer printed wiring board according to claim 25, [comprising build-up wiring layers including the at least one via-hole provided in the at least

one interlaminar resin insulating layer] wherein the at least one interlaminar resin insulating layer comprises a plurality of interlaminar resin insulating layers, the plurality of interlaminar resin insulating layers and at least one via-hole provided in the interlaminar resin insulating layers form build-up wiring layers, and the build-up wiring layers are formed on both surfaces of the substrate[, and have the same number of layers [with each other] on both surfaces of the substrate.

Claim 30 (amended): A multilayer printed wiring board comprising:  
a substrate [provided with] having at least one through-hole structure, [the substrate having] the at least one through-hole structure being filled with filler;  
at least one interlaminar resin insulating layer formed [thereon] on the substrate; and  
at least one conductor circuit formed on the at least one interlaminar resin insulating layer[, the at least one through-hole being filled with filler],  
wherein an internal surface of the at least one through-hole structure is roughened,  
and the filler comprises particulate substance having a particle size of from 0.1 to 30  $\mu\text{m}$ ,  
resin, and ultrafine inorganic powder having a particle size from [1 to 1000] 2 to 100 nm, and  
an exposed surface of the filler in the at least one through-hole structure is covered with a  
[portion of the at least one conductor circuit] through-hole-covering conductor layer, and at  
least one viahole is formed in the at least one interlaminar resin insulating layer [just] directly  
above the [at least one conductor circuit and is connected to the at least one conductor circuit]  
through-hole-covering conductor layer.

Claim 31: The multilayer printed wiring board according to claim 30, wherein the filler is a nonconducting composition containing metal particles.

Claim 32: The multilayer printed wiring board according to claim 30, wherein the particulate substance comprises at least one of metal particles, inorganic particles and resin particles.

Claim 33: The multilayer printed wiring board according to claim 30, wherein the resin comprises at least one of bisphenol epoxy resin and novolac epoxy resin.

Claim 34 (amended): The multilayer printed wiring board according to claim 30, wherein [a roughened layer is formed on] a surface of the [at least one conductor circuit covering the at least one through-hole] through-hole-covering conductor layer is roughened.

Claim 35: The multilayer printed wiring board according to claim 30, wherein the substrate is a multilayer core substrate formed by laminating at least one conductor layer and at least one prepreg in alternating order.

Claim 36 (amended): The multilayer printed wiring board according to claim 30, wherein the least one through-hole structure formed [on] in the substrate has a pitch interval of equal to or less than 700  $\mu\text{m}$ .

Claim 37 (amended): The multilayer printed wiring board according to claim 30, [comprising build-up wiring layers including the at least one via-hole provided in the at least one interlaminar resin insulating layer] wherein the at least one interlaminar resin insulating layer comprises a plurality of interlaminar resin insulating layers, the plurality of interlaminar resin insulating layers and at least one via-hole provided in the interlaminar resin insulating layers form build-up wiring layers, and the build-up wiring layers are formed on both surfaces of the substrate[,], and have the same number of layers [with each other] on both surfaces of the substrate.

Claim 38 (amended): A resin composition for filling through-hole of a printing wiring board comprising:

particulate substance comprising metal powder having an average particle size ranging from 0.1 to 30  $\mu\text{m}$  and being present in an amount ranging from 30 to 90% by weight of the total solids content of the resin composition[,];

resin and



ultrafine inorganic powder having an average particle size ranging from [1 to 1,000] 2 to 100 nm.

Claim 39 (amended): The resin composition according to claim 38, which is a nonconducting composition.

Claim 40 (amended): The resin composition according to claim 38, wherein the particulate substance comprises at least one member selected from the group consisting of metal particulate, inorganic particles [or] and resin particles.

Claim 41: The resin composition according to claim 38, wherein the resin comprises at least one of bisphenol epoxy resin and novolac epoxy resin.

Claim 42: The resin composition according to claim 41, wherein the bisphenol epoxy resin comprises at least one of bisphenol P epoxy resin and bisphenol A epoxy resin.

Claim 43: The resin composition according to claim 41, wherein the novolac epoxy resin comprises at least one of phenol novolac epoxy resin and cresol novolac epoxy resin.

Claim 44: The resin composition according to claim 41, wherein the composition ratio of the novolac epoxy resin to the bisphenol epoxy resin ranges from 1/1 to 1/100 by weight.

Claim 45: The resin composition according to claim 38, wherein the ultrafine inorganic powder is present in an amount ranging from 0.1 to 5% by weight of the total solids content of the resin composition and has an average particle size ranging from 2 to 200 nm.

Claim 46 (amended): The resin composition according to claim 38, wherein the ultrafine inorganic powder [is] comprises at least one material selected from the group consisting of silica, alumina, silicon carbide [or] and mullite.

Claim 47: The resin composition according to claim 46, wherein the ultrafine inorganic powder is silica.

Claim 48 (amended): A process of producing a multilayer printed wiring board comprising:

forming a hole in a substrate;

[forming at least one conductor layer on both surfaces of a substrate by electroless plating,]

forming [at least one] a through-hole structure [on] in the substrate, the forming including plating a layer on a surface of the hole;

[forming a roughened layer on] roughening [an internal] a surface of a plated layer of the [at least one] through-hole structure;[,]

filling the [at least one] through-hole structure including the plated layer having [the] a roughened [layer on its internal] surface with filler comprising metal particles and one of thermosetting and thermoplastic resin[, and drying and curing the filler,]

forming a first conductor layer having a first conductor circuit on the substrate;

forming [at least one] a first interlaminar resin insulating layer on the first conductor circuit and the substrate;[, and]

forming a via hole in the interlaminar resin insulating layer; and

forming [at least one] a second conductor layer having a second conductor circuit [by electroless plating] on the first interlaminar resin insulating layer,

wherein the via hole is formed to connect the first conductor circuit and the second conductor circuit.

Claim 49 (amended): The process according to claim 48, wherein the [internal] surface of the plated layer of the [at least one] through-hole structure is roughened by a treatment selected from the group consisting of an oxidation-reduction treatment, a treatment with an aqueous mixed solution of an organic acid and a copper (II) complex, [or] and a plating treatment with a needle ternary alloy of copper-nickel-phosphorous.

Cancel Claim 50.

Claim 51 (amended): The process according to claim 48, wherein forming the [at least one conductor circuit] first conductor circuit and the second conductor circuit comprises electroplating after electroless plating.

Claim 52 (amended): A process of producing a multilayer printed wiring board, comprising:

forming a hole in a substrate;

[forming at least one conductor layer on both surfaces of a substrate by electroless plating,]

forming [at least one] a through-hole structure [through] in the substrate, the forming including plating a layer on a surface of the hole;

[forming a roughened layer on] roughening [an internal] a surface of a plated layer of the [at least one] through-hole structure;[,]

filling the [at least one] through-hole structure including the plated layer having [the] a roughened [layer on its internal] surface with filler comprising particulate substance including metal particles having a particle size of from 0.1 to 30  $\mu\text{m}$ , resin, and ultrafine inorganic powder having a particle size from [1 to 1000] 2 to 100 nm[, and drying and curing the filler,];

forming a first conductor layer having a first conductor circuit on the substrate;

forming [at least one] a first interlaminar resin insulating layer on the first conductor circuit and the substrate;[, and]

forming a via hole in the first interlaminar resin insulating layer; and

forming [at least one] a second conductor layer having a second conductor circuit [by electroless plating] on the first interlaminar resin insulating layer,

wherein the via hole is formed to connect the first conductor circuit and the second conductor circuit.

Claim 53 (amended): The process according to claim 52, wherein the filler is a nonconducting composition [containing metal particles].

Claim 54 (amended): The process according to claim 52, wherein the particulate substance comprises at least one of [metal particles,] inorganic particles and resin particles.

Claim 55: The process according to claim 52, wherein the resin comprises at least one of bisphenol epoxy resin and novolac epoxy resin.

Claim 56 (amended): The process according to claim 52, wherein forming the [at least one] first conductor layer and the second conductor layer comprises electroplating after electroless plating.

Claim 57 (amended): The process according to claim 52, wherein forming the [at least one] first conductor circuit and the second conductor circuit comprises electroplating after electroless plating.

Cancel Claims 58-66.

Claim 67 (amended): The process according to claim [66] 52, wherein the filler is a nonconducting composition having a specific resistance of equal to or more than  $1 \times 10^6$  [ $\Omega \cdot \text{cm}^2$ ]  $\Omega \cdot \text{cm}$  and containing metal particles.

Claim 68 (amended): The process according to claim [67] 52, wherein the particulate substance comprises at least one of metal particles, inorganic particles and resin particles.

Cancel Claims 69 and 70.

Claim 71 (amended): The process according to claim [66] 52, wherein the forming of the first conductor layer includes subjecting a portion of the filler in the through-hole to electroless plating [wherein forming the portion of the at least one conductor layer on the at

least one through-hole comprises] and electroplating [after electroless plating] to cover the through-hole.

Claim 72 (amended): A process of producing a multilayer printed wiring board comprising:

forming a hole in a substrate;

[forming at least one conductor layer on both surfaces of a substrate by electroless plating,]

forming [at least one] a through-hole structure [on] in the substrate, the forming includes plating a layer on a surface of the hole;

[forming a roughened layer on] roughening [an internal] a surface of a plated layer of the [at least one] through-hole[,] structure;

filling the [at least one] through-hole structure including the plated layer having [the] a roughened [layer on its internal] surface with filler comprising metal particles and one of the thermosetting and thermoplastic resin[, and drying and curing the filler,];

forming a [portion of the at least one] first conductor layer having a through-hole-covering conductor layer on the [at least one] through-hole structure [by subjecting a portion of the filler on the at least one through-hole to electroless plating,];

forming [at least one] a first interlaminar resin insulating layer[,] on the first conductor layer; and

forming at least one viahole in the first interlaminar resin insulating layer and [at least one] a second conductor circuit [in] on the [at least one] first interlaminar resin insulating layer, [located just above the at least one through-hole, and]

wherein the at least one viahole is formed at a position directly above the through-hole structure and provided to connect the through-hole-covering conductor layer with the second conductor circuit

[connecting the at least one viahole to the at least one conductor circuit in the at least one interlaminar resin insulating layer located just above the at least one through-hole].

Claim 73 (amended): The process according to claim 72, wherein the [internal] surface of the plated layer of the [at least one] through-hole structure is roughened by a treatment selected from the group consisting of oxidation-reduction treatment, treatment with an aqueous mixed solution of an organic acid and a copper (II) complex, [or] and plating treatment with needle ternary alloy of copper-nickel-phosphorus.

Claim 74 (amended): The process according to claim 72, wherein the forming the [portion of the at least one conductor layer] through-hole-covering conductor layer on the [at least one] through-hole structure comprises smoothing a surface of the substrate, applying catalyst nuclei to the smoothed surface of the substrate, subjecting the substrate to electroless plating to form a plating layer, subjecting the substrate to electroplating, forming an etching resist [just] directly above the [at least one] through-hole structure and on a portion of the [at least one] through-hole structure [and the plating layer which is to become a part of the at least one conductor circuit], removing the plating layer in a portion of the substrate where the etching resist is not formed, and removing the etching resist.

Claim 75 (amended): The process according to claim 72, wherein the forming the [portion of the at least one conductor layer] through-hole-covering conductor layer on the [at least one] through-hole structure comprises smoothing a surface of the substrate, subjecting the substrate to electroless plating to form a plating layer, forming a plating resist on [a part of the smoothed surface of the substrate] the plating layer, subjecting [a portion of the smoothed surface of] the substrate to electroplating [where the resist is not formed to electroplating to form the at least one conductor layer and the at least one conductor circuit], [and] removing the plating resist, and [with] etching the [at least one conductor layer] plating

layer located beneath the plating resist [by etching] to form the through-hole-covering conductor layer.

Claim 76 (amended): The process according to claim 72, wherein the forming the [portion of the at least one conductor layer] through-hole-covering conductor layer on the [at least one] through-hole comprises roughening a surface of the portion of the [at least one conductor layer] through-hole-covering conductor layer by a treatment selected from the group consisting of oxidation-reduction treatment, treatment with an aqueous mixed solution of an organic acid and a copper (II) complex, [or] and plating treatment with needle ternary alloy of copper-nickel-phosphorus.

Cancel Claims 77 and 78.

Claim 79 (amended): The process according to claim 72, wherein forming [at least one] the first conductor layer on both surfaces of [a] the substrate comprises electroplating after electroless plating.

Claim 80 (amended): The process according to claim 72, wherein forming [a portion of the at least one conductor layer] through-hole-covering conductor layer on the [at least one] through-hole structure comprises electroplating after electroless plating.

Claim 81 (amended): A process of producing a multilayer printed wiring board comprising:

forming a hole in a substrate;

[forming at least one conductor layer on both surfaces of a substrate by electroless plating,]

forming [at least one] a through-hole structure [on] in the substrate, the forming including plating a layer on a surface of the hole;

[forming a roughened layer on] roughening [an internal] a surface of a plated layer of the [at least one] through-hole structure.

filling the [at least one] through-hole structure including the plated layer having [the] a roughened [layer on its internal] surface with filler comprising particulate substance having a particle size of from 0.1 to 30  $\mu\text{m}$ , resin, and ultrafine inorganic powder having a particle size from [1 to 1000] 2 to 100 nm[, and drying and curing the filler,];

forming a [portion of the at least one] first conductor layer having a through-hole-covering conductor layer on the [at least one] through-hole structure; [by subjecting a portion of the filler on the at least one through-hole structure to electroless plating,]

forming [at least one] a first interlaminar resin insulating layer[,]; and

forming at least one viahole in the first interlaminar resin insulating layer and [at least one] a second conductor circuit [in] on the [at least one] first interlaminar resin insulating layer, [located just above the at least one through-hole, and]

wherein the viahole is formed at a position directly above the through-hole structure and provided to connect the through-hole-covering conductor layer with the second conductor circuit

[connecting the at least one viahole to the at least one conductor circuit in the at least one interlaminar resin insulating layer located just above the at least one through-hole].

Claim 82: The process according to claim 81, wherein the filler is a nonconducting composition and further comprises metal particles.

Claim 83: The process according to claim 82, wherein the particulate substance comprises at least one of metal particles, inorganic particles and resin particles.

Claim 84: The process according to claim 82, wherein the resin comprises at least one of bisphenol epoxy resin and novolac epoxy resin.

Claim 85 (amended): The process according to claim 82, wherein forming the [at least one] first conductor layer comprises electroplating after electroless plating.



Claim 86 (amended): The process according to claim 82, wherein forming the [portion of the at least one] first conductor layer on the [at least one] through-hole structure comprises electroplating after electroless plating.

Claim 87 (amended): A multilayer printed wiring board comprising:  
a substrate having a through-hole structure comprising a plating layer and a filler  
provided in the through-hole structure, the plating layer having a roughened portion;  
a first conductor layer having a first conductor circuit formed on the substrate and a  
through-hole-covering conductor layer covering the filler provided in the through-hole  
structure having the plating layer;  
a first interlaminar resin insulating layer having a via hole and being formed on the  
substrate and the first conductor layer; and  
a second conductor layer having a second conductor circuit formed on the first  
interlaminar resin insulating layer, the second conductor circuit being connected to the first  
conductor circuit by the via hole.

Claim 88 (previously presented): The multilayer printed wiring board according to Claim 87, wherein said via hole is filled with a plated film or a filler.

Claim 89 (amended): The multilayer printed wiring board according to Claim 87,  
wherein a surface of said through-hole-covering conductor layer is roughened.

Claim 90 (amended): The multilayer printed wiring board according to Claim 89,  
wherein a side face of said through-hole-covering conductor layer is roughened.

Claim 91 (previously presented): The multilayer printed wiring board according to Claim 87, further comprising:

a roughened layer provided in said at least one through-hole and having the roughened internal surface, a thickness of the roughened layer being at least 0.1  $\mu\text{m}$  and at most 10  $\mu\text{m}$ .

Claim 92 (previously presented): The multilayer printed wiring board according to Claim 87, wherein said substrate comprises a glass-epoxy substrate, a polyimide substrate, a bismaleimide-triazine resin substrate, a fluororesin substrate, a copper-clad laminate resin substrate, a ceramic substrate, or a metal substrate.

Claim 93 (new): The multilayer printed wiring board according to Claim 1, wherein the filler is non-conductive.

Claim 94 (new): The multilayer printed wiring board according to Claim 12, wherein the filler is non-conductive.

Claim 95 (new): The multilayer printed wiring board according to Claim 25, wherein the filler is non-conductive.

Claim 96 (new): The process according to Claim 48, wherein the forming of the first conductor layer comprises forming a through-hole-covering conductor layer which covers the filler.

Claim 97 (new): The process according to Claim 96, wherein the via hole is formed on the through-hole-covering conductor layer and located directly over the filler.

Claim 98 (new): The process according to Claim 48, wherein the filler is a nonconductive composition.

Claim 99 (new): The process according to Claim 48, wherein the substrate comprises copper-clad laminate, and the filler protruded from the through-hole structure is removed by polishing.

Claim 100 (new): The process according to Claim 48, wherein the forming of the first conductor layer comprises forming a through-hole-covering conductor layer to cover the filler, and the forming of the through-hole-covering conductor layer comprises performing electroless plating and electroplating after the electroless plating.

Claim 101 (new): The process according to Claim 52, wherein the forming of the first conductor layer includes forming a through-hole-covering conductor layer which covers the filler.

Claim 102 (new): The process according to Claim 101, wherein the via hole is formed on the through-hole-covering conductor layer and located directly over the filler.

Claim 103 (new): The process according to Claim 52, wherein the substrate is copper-clad laminate and the filler protruded from the through-hole structure is removed by polishing.

Claim 104 (new): The process according to Claim 52, wherein the forming of the first conductor layer includes forming a through-hole-conductor layer which covers the filler, and the forming of the through-hole-conductor layer includes performing electroless plating and electroplating after the electroless plating.

Claim 105 (new): The multilayer printed wiring board according to Claim 87, wherein the via hole is formed on the through-hole-covering conductor layer.

Claim 106 (new): The multilayer printed wiring board according to Claim 87, wherein the via hole is formed on the through-hole-covering conductor layer, and the via hole is formed above the filler.

Claim 107 (new): The multilayer printed wiring board according to Claim 87, wherein the through-hole-covering conductor layer comprises an electroless plating film and an electroplating film on the electroless plating film.

Claim 108 (new): The multilayer printed wiring board according to Claim 87, wherein the filler comprises metal particles.

Claim 109 (new): The multilayer printed wiring board according to Claim 108, wherein the filler is non-conductive.

Claim 110 (new): A process of producing a multilayer printed wiring board comprising:

forming a hole in a substrate;

forming a through-hole structure in the substrate, the forming including plating a layer on a surface of the hole;

roughening a portion of a plating layer of the through-hole structure;

filling a filler inside the through-hole structure;

forming a first conductor layer having a first conductor circuit on the substrate and a through-hole-covering conductor layer covering the filler by plating;

forming a first interlaminar resin insulating layer on the conductor circuit and substrate;

forming a via hole in the interlaminar resin insulating layer; and

forming a second conductor layer having a second conductor circuit on the first interlaminar resin insulating layer,

wherein the via hole is formed to connect the first conductor circuit and the second conductor circuit.

Claim 111 (new): The process according to Claim 110, wherein the via hole is formed on the through-hole-covering conductor layer at a position directly above the filler.

Claim 112 (new): The process according to Claim 110, wherein the filler comprises metal particles and one of thermosetting and thermoplastic resin.